MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2017/2018

EEE1046 – ELECTRONICS III

(All sections / Groups)

30- MAY 2018
09:00 AM – 11:00 AM
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 5 pages (including the cover page) with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1

(a) Operational amplifier (Op-amp) circuits with external negative feedback are widely used for a variety of applications, such as the summing amplifiers.

(i) Explain the term *negative feedback*. Next, give **TWO** advantages of the negative feedback configuration in an op-amp circuit. [2+2 marks]

(ii) Sketch the schematic diagram of an ideal inverting summing amplifier circuit that has **THREE** inputs. Label the series input resistors (R_1, R_2, R_3), feedback resistor (R_F), input voltages (V_{IN1}, V_{IN2}, V_{IN3}), and output voltage (V_{OUT}) accordingly. [4 marks]

(iii) With the aid of the sketch in Part (a)(ii), derive the mathematical expression for the output voltage V_{OUT} of the ideal inverting summing amplifier. [4 marks]

(iv) The ideal inverting summing amplifier circuit in Part (a)(ii) has unity gain. The waveforms of input signals V_{IN1}, V_{IN2} and V_{IN3} are shown in Figure Q1(a). Draw the graph of the output waveform. [3 marks]

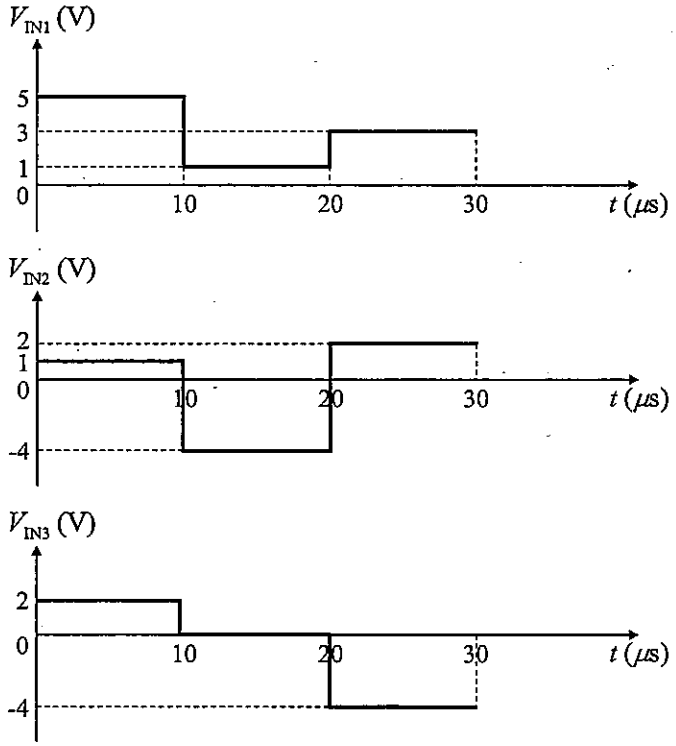

Figure Q1 (a)

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(b) Figure Q1(b) shows the schematic diagram of an ideal op-amp integrator circuit, which simulates mathematical integration by determining the total area under the curve of a function. A square wave as shown in Figure Q1(c) is applied to the input of the differentiator.

(i) The integrator has $C_F = 1$ nF and $R_1 = 10$ kΩ. Determine the output voltage V_o at time $t = 0$ s, $t = 2$ μs, $t = 5$ μs, $t = 10$ μs. [5 marks]

(ii) At low frequencies, the ideal integrator circuit may become unstable and drive the output signal into saturation. Explain why? [3 marks]

(iii) Suggest a modification to the ideal integrator circuit to eliminate the instability. [2 marks]

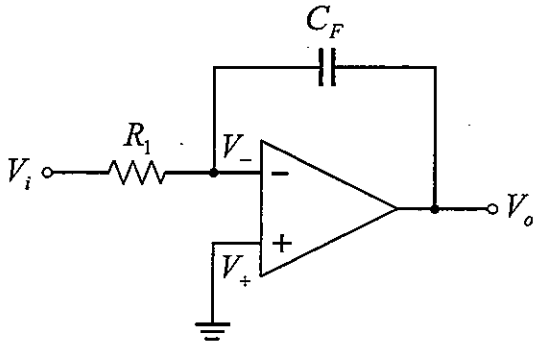

Figure Q1 (b)

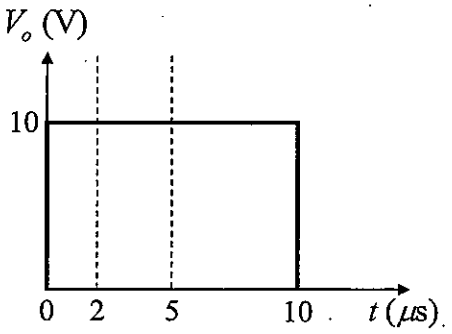

Figure Q1 (c)

Question 2

(a) List and describe the **THREE** main stages which form the internal structure of an integrated circuit (IC) op-amp. [6 marks]

(b) The output voltage V_0 of an operational amplifier is 2.002 V when $V_+ = 1005$ μV and $V_- = 995$ μV. When $V_+ = 1010$ μV and $V_- = 1000$ μV, V_0 is 2.00201 V. Calculate the open loop gain A_{OL} and common-mode rejection ratio (in decibels) of the amplifier. [6 marks]

(c) The slew rate of the amplifier in Figure Q2(c) is 0.5 V/μs.

(i) Is this an inverting or a non-inverting amplifier? [1 mark]

(ii) Calculate the maximum frequency supported by the circuit for the case when $R_L = 6$ kΩ. Find out the maximum peak input voltage allowable. [4 marks]

(iii) What are the new maximum frequency and maximum peak input voltage supported by the circuit if R_L is changed to 16 kΩ? [4 marks]

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(iv) With the aid of a diagram, explain what will happen to the output of the circuit if the input exceeds the slew rate of 0.5 V/μs. [4 marks]

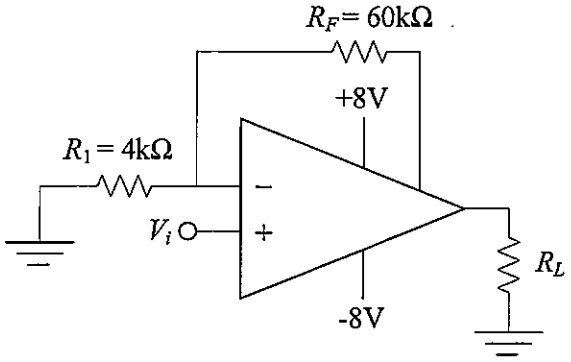

Figure Q2 (c)

Question 3

(a) A simple shunt regulator is shown in Figure Q3 (a).

(i) Derive the appropiate equation for V_Z , I_S , I_L and I_Z for this circuit and explain the weakness of this circuit. [3 marks]
Sketch the **improved version** of this shunt regulator circuit. Derive appropiate equation for V_Z , I_S , I_L and other related equations for this improved circuit. And explain the advantage of the improved circuit over the circuit shown in Figure Q3(a). [5 marks]

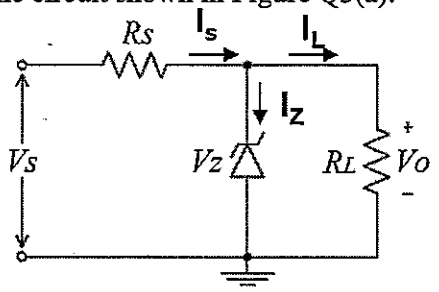

Figure Q3 (a)

(b) Given the value of the series regulator circuit shown in Figure Q3(b) are V_i = 15V, V_Z = 8.3V, R_1 = 100 Ω, R_2 = 50 kΩ and R_3 = 150 kΩ. Assume the op-amp used in Figure Q3(b) is ideal.

(i) Determine the value of regulated voltage, V_o and the circuit currents, I_Z and I_{R2}. [8 marks]

(ii) Determine the power dissipation of the pass transistor if Vo is connecting to an external load circuit which draws 100mA. [3 marks]

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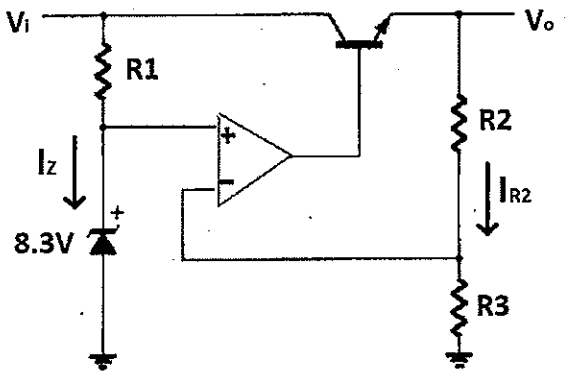


Figure Q3(b)

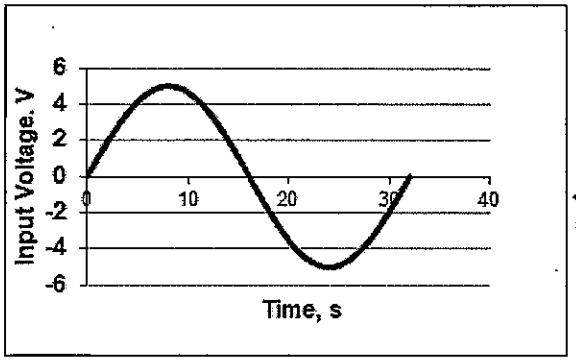
(iii) Sketch a Hartley oscillator circuit that operates at frequency 1.5MHz with its $|\beta| = 0.4$. Determine its inductors value if you are given a capacitor value $C = 0.5$ pF. Assume the op-amp in your circuit is ideal and the resistance of the resistor that connected to the inductor is much higher than the inductance value at the operating frequency. [6 marks]

Question 4

(a) A first order Low-Pass Filter (1st Order LP) and is followed by a first order High-Pass Filter (1st Order HP) is the constructed filter. Assume $K_{HP} = K_{LP}$. Design a wide band pass filter with approximately constant pass-band gain for $f_c = 3$ kHz, $BW = 1$ kHz and $K_{PB} = 4$. [17 marks]

(b) Figure Q4 (b) is a bounded comparator. Determine the output voltage, V_o values for the input voltage, Vi. Then, draw the output voltage, V_o timing waveform with respect to the input voltage, Vi timing waveform as shown in the figure Q4 (b).

[8 marks]



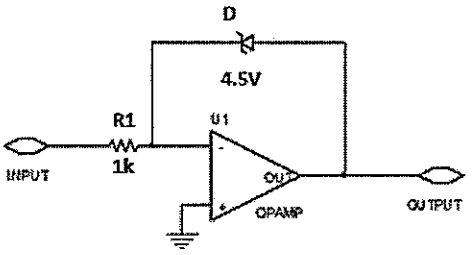


Figure Q4(b)

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